11/09/00

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventorship ..... Sidiropoulos et al.
Applicant..... Rambus Inc.
Attorney's Docket No. RB1-005US
Title: Reducing Coupled Noise in Pseudo-Differential Signaling Systems

TRANSMITTAL LETTER AND CERTIFICATE OF MAILING

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

From: Daniel L. Hayes (509) 324-9256
Lee & Hayes, PLLC
421 W. Riverside Avenue, Suite 500
Spokane, WA 99201

The following enumerated items accompany this transmittal letter and are being submitted for the matter identified in the above caption.

1. Transmittal Letter with Certificate of Mailing included.
2. PTO Return Postcard Receipt
3. Check in the Amount of $1,916
4. Fee Transmittal
5. New patent application (title page plus 31 pages, including claims 1-67 & Abstract)
6. Executed Declaration
7. 4 sheets of formal drawings (Figs. 1-7)
8. Assignment w/Recordation Cover Sheet

Large Entity Status [x] Small Entity Status [ ]

The Commissioner is hereby authorized to charge payment of fees or credit overpayments to Deposit Account No. 12-0769 in connection with any patent application filing fees under 37 CFR 1.16, and any processing fees under 37 CFR 1.17.

Date: 11/7/00 By: Daniel L. Hayes
Daniel L. Hayes
Reg. No. 34,618

CERTIFICATE OF MAILING

I hereby certify that the items listed above as enclosed are being deposited with the U.S. Postal Service as either first class mail, or Express Mail if the blank for Express Mail No. is completed below, in an envelope addressed to The Commissioner of Patents and Trademarks, Washington, D.C. 20231, on the below-indicated date. Any Express Mail No. has also been marked on the listed items.

Express Mail No. (if applicable) EL685270387

Date: Nov. 7, 2000 By: Helen M. Hare
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FEE TRANSMITTAL for FY 2001

Patent fees are subject to annual revision

TOTAL AMOUNT OF PAYMENT ($) 1,916 ^00

Complete if Known	
Application Number	
Filing Date	
First Named Inventor	Sidiropoulous et al.
Examiner Name	
Group Art Unit	
Attorney Docket No.	RBI-005US

METHOD OF PAYMENT

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to

Deposit Account Number: 12-0769

Deposit Account Name: Lee & Hayes, PLLC

[X] Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

[ ] Applicant claims small entity status. See 37 CFR 1.27

2. [X] **Payment Enclosed:**

[X] Check [ ] Credit card [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	710	201	355	Utility filing fee	710
106	320	206	160	Design filing fee	
107	490	207	245	Plant filing fee	
108	710	208	355	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 710^00

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below	= Fee Paid
Total Claims	67	-20** =	47	X	18	= 846
Independent Claims	7	- 3** =	4	X	80	= 320
Multiple Dependent						=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	80	202	40	Independent claims in excess of 3
104	270	204	135	Multiple dependent claim, if not paid
109	80	209	40	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 1166^00

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	390	216	195	Extension for reply within second month	
117	890	217	445	Extension for reply within third month	
118	1,390	218	695	Extension for reply within fourth month	
128	1,890	228	945	Extension for reply within fifth month	
119	310	219	155	Notice of Appeal	
120	310	220	155	Filing a brief in support of an appeal	
121	270	221	135	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,240	241	620	Petition to revive - unintentional	
142	1,240	242	620	Utility issue fee (or reissue)	
143	440	243	220	Design issue fee	
144	600	244	300	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	40
146	710	246	355	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	710	249	355	For each additional invention to be examined (37 CFR § 1.129(b))	
179	710	279	355	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	

Other fee (specify) _____

* Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 40^00

SUBMITTED BY				Complete *(if applicable)*	
Name (Print/Type)	Daniel L. Hayes	Registration No. (Attorney/Agent)	34,618	Telephone	(509) 324-9256
Signature	Daniel L. Hayes			Date	11/7/00

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

Reducing Coupled Noise in Pseudo-Differential Signaling Systems

Inventors:
Stefanos Sidiropoulos
Ying Li
Mark A. Horowitz

ATTORNEY'S DOCKET NO. RB1-005US

TECHNICAL FIELD

The present invention relates to the transmission of data over transmission lines that are subject to capacitively and/or inductively coupled noise. More specifically, the present invention reduces the effect of such induced or coupled noise in systems using pseudo-differential transmission lines.

BACKGROUND

Fig. 1 shows an electronic system that transmits data or other signals using pseudo-differential signaling. The system includes a first integrated circuit 10 that transmits the signals, and a second integrated circuit 12 that receives the signals. The signals comprise voltages that are conducted between the two integrated circuits by a plurality of signal lines 14. The signal lines are typically metallic traces on a printed circuit board.

In addition to the signals themselves, a reference voltage is transmitted from first integrated circuit 10 to second integrated circuit 12, over a reference line 16. The signal voltages represent values in terms of relationships between the signal voltages and the reference voltage. In a binary system, for example, a high voltage—one which is higher than the reference voltage—might represent a binary "1". A low voltage—one that is less than the reference voltage—might represent a binary "0".

Fig. 2 illustrates how the values of signal lines are determined within the receiving integrated circuit 12. A signal comparator 20, often in the form of a comparator, is associated with each signal voltage V_{SIG}. Each signal line is routed to a first input of the associated signal comparator 20. The reference voltage V_{REF} is routed in common to the second input of each signal comparator 20. The signal

comparator produces a high logic level within integrated circuit 12 if the signal voltage is higher than the reference voltage. The signal comparator produces a low logic level within integrated circuit 12 if the signal voltage is not higher than the reference voltage.

This type of signaling technique reduces or cancels the effect of any electrical noise that is induced in signal lines 14 between the two integrated circuits. The technique works on the assumption that any noise induced in a signal line will be similarly induced in the common reference line. This assumption, in turn, relies on the further assumption that the signal lines are subject to the same noise inducing influences as the reference line.

These assumptions are generally correct, at least to a degree. In high-speed data transfer circuits, however, it is often desired to utilize very small differentials between "high" and "low" signal voltages. The use of such small voltage differentials accentuates the effect of any differences in induced noise between the signal lines and the reference line.

In sensitive circuits such as these, even small differences in induced noise can become significant. One reason such differences arise is that the reference line is routed to many more components than an individual signal line. Specifically, a signal line is routed (within the receiving integrated circuit) to only a single signal comparator. The reference line, on the other hand, is routed to all of the signal comparators. Each connection to signal comparator introduces a new source of noise coupling. Furthermore, additional routing lengths are usually required to reach the signal comparators, which also adds coupling capacitance.

Fig. 3 shows a simplified model of a reference line 30 and a signal line 32. The lines are driven by devices having equal output impedances, and the

transmission lines are carefully designed to have the same distributed line impedances. The transmission line and driver impedances are represented as R_C in Fig. 3.

At the receiving integrated circuit, the reference line and signal line are connected to a package pin. This pin introduces a parasitic inductance L_I. Within the integrated circuit, both of the lines are capacitively coupled to the substrate (V_{SS}) of the integrated circuit. This coupling is mainly through the capacitances of the input pad, existing electrostatic discharge (ESD) circuitry, and the inputs of the signal comparators. Since the reference line drives a multitude of signal comparators and has a longer routing path, its coupling capacitance C_{REF} is significantly larger than the capacitance C_{IN} of the signal line. Moreover, depending on the length and the resistivity of the reference routing wire, the additional capacitance of the reference line may behave as a distributed RC line.

The capacitive coupling C_{REF} and C_{IN} result in noise injection from the integrated circuit's power supply rails to the signal and reference lines. If C_{REF} and C_{IN} were equal, the noise injection would be common mode and would not affect the interpretation of the signal. But because C_{REF} is so much greater than C_{IN} in a pseudo-differential interface, the noise injection on the reference line is fundamentally larger than that on the signal line. This results in a reduction of common mode noise rejection by the signal comparators, especially at high frequencies.

The technique described below reduces the effect of noise injection in pseudo-differential interfaces such as shown in Figs. 1-3.

SUMMARY

In the circuits described below, the reference voltage is buffered in the receiving circuit prior to its distribution to the multiple signal comparators. In one embodiment, the buffered voltage is the sum of the reference voltage and its noise. In another embodiment, the buffered voltage represents only the noise.

The buffered voltage is used in each embodiment to account for the differences between impedances seen by the signal voltages and the relatively greater impedances seen by the reference voltage.

In one embodiment, the buffering is accomplished with an active buffer such as a unity gain operational amplifier, having a bandwidth that is significantly greater than the resonant input frequency of the reference and signal inputs.

Alternatively, both the signal voltages and the reference voltages are buffered using MOSFET source-followers. To reduce differential noise injection, the source-follower associated with the reference input is larger than the source-follower of the signal inputs by specific ratio. This ratio is equal to the ratio of the capacitance seen by the output of the source-follower associated with the reference line to the capacitance seen by the output of the source-follower associated with the signal line.

In another embodiment, the buffered voltage represents only the noise of the signal lines, and is subtracted from the signal voltages to remove the noise.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates a prior art pseudo-differential signaling system.

Fig. 2 illustrates receiving circuitry of a prior art pseudo-differential signaling system.

Fig. 3 illustrates electrical characteristics of signal and reference lines in a prior art pseudo-differential signaling system.

Fig. 4 illustrates a pseudo-differential signaling system in which the invention can be embodied.

Fig. 5 illustrates electrical characteristics of a receiving circuit in a pseudo-differential signaling system.

Figs. 6 and 7 illustrate electrical characteristics of receiving circuits in alternative embodiments of pseudo-differential signaling systems.

DETAILED DESCRIPTION

Fig. 4 shows a system 100 including a first integrated circuit 102 that transmits pseudo-differential data signals in conjunction with a reference signal, and a second integrated circuit 104 that receives the data and reference signals. Specifically, the signals include a plurality of pseudo-differential data signal voltages, referred to herein simply as signal voltages, and a single, common reference voltage. These signals are conducted on corresponding pseudo-differential signal lines 106 and a reference line 108.

The pseudo-differential data signals represent values in terms of relationships between the signal voltages and the common reference voltage. In the described embodiment, for example, a signal voltage that is higher than the reference voltage represents a binary "1". A data signal voltage that is lower than the reference voltage represents a binary "0".

Fig. 5 shows receiver circuitry, within receiving integrated circuit 104, corresponding to the reference signal and one of the signal lines. Parasitic inductance L_I is introduced on each signal line by the corresponding package pins

on the integrated circuit—the external pins to which the lines are routed from the transmitting integrated circuit.

Each signal line is routed within integrated circuit 104 to a signal receiver or comparator 110. Integrated circuit 104 has a plurality of such signal comparators, corresponding respectively to each of the received pseudo-differential signals.

With regard to the data signal lines, coupling capacitance is represented as C_S. Noise is injected into each data signal line from the integrated circuit's substrate V_{SS} through coupling capacitance C_S. C_S is a result of capacitances of the input pad corresponding to the signal line, existing ESD circuitry, and the input of the data signal comparator 110.

The reference voltage or signal is routed within the integrated circuit to a reference receiver 112, before the reference voltage has been distributed to the various signal comparators. In this embodiment, the reference receiver is an active buffer. More specifically, reference receiver 112 is a unity gain amplifier—preferably an operational amplifier—that receives the common reference voltage and in response produces a buffered common reference voltage or signal V_{BUF}, also referred to herein as a buffered signal or voltage. The buffered voltage is distributed to each of data signal comparators 110. Thus, each data signal comparator compares or otherwise evaluates the buffered reference voltage and the corresponding pseudo-differential signal voltage to determine the value represented by the signal voltage.

In the described embodiment, each signal comparator comprises a transistor-based comparator that compares two input voltages and produces a

binary voltage output that is dependent on which of the two input voltages is greater. Optionally, the voltage output might be produced as a differential signal.

With regard to the reference line, coupling capacitance includes C_{R1} and C_{R2}. C_{R1} represents coupling capacitance of the *unbuffered*, undistributed, common reference signal, and is a result of capacitances of the input pad corresponding to the reference line, ESD circuitry, and the input of active buffer 112. Noise is injected into the unbuffered reference line from the integrated circuit's substrate V_{SS} through coupling capacitance C_{R1}. Active buffer 112 is designed to have an input capacitance approximately equal to the input capacitance of any one of the data signal comparators 110 and also to equal C_{R1}. This ensures that integrated circuit 104 presents similar input impedances to both the unbuffered reference voltage and the multiple signal voltages.

C_{R2} represents coupling capacitance of the *buffered* reference signal. This capacitance is due primarily to the combined capacitances of the inputs of the multiple signal comparators 110. Active buffer 112 is designed with a large enough bandwidth to minimize the effects of C_{R2} and to thereby minimize any noise injection through C_{R2}.

In the circuit of Fig. 5, noise induced by capacitive coupling in the receiving integrated circuit will be largely common mode, since C_S equals C_{R1} and since active buffer 112 has a sufficient bandwidth to largely negate any significant noise injection through C_{R2}. In practice, active buffer 112 should have a bandwidth that is significantly greater than the resonant input frequency of the data signal line—a function of L_I and C_S. Specifically, the bandwidth of active buffer 112 should be at least ten times greater than the resonant input frequency of the data signal lines.

This circuit arrangement ensures that approximately equal coupled signal noise is introduced in the distributed reference voltage and the plurality of pseudo-differential signal voltages. Such common mode noise is canceled in the comparisons performed by the signal comparators.

The described technique has been found to be extremely practical and beneficial, especially in integrated circuits running at higher clock speeds and having higher values of L_I.

Fig. 6 illustrates an alternative embodiment in which both the signal voltages and the reference voltage are buffered. Specifically, the receiving integrated circuit has a plurality of receivers or active buffers 202 that receive the pseudo-differential signal voltages and in response produce buffered signal voltages. Similarly, the reference voltage is routed to a single receiver or active buffer 204 that produces a buffered reference voltage. The buffers need not have a unity gain, but they do have approximately identical gains. In the described embodiment, they are MOSFET-based source-followers.

Coupling capacitance associated with the signal voltage includes C_{S1} and C_{S2}. C_{S1} represents coupling capacitance of the *unbuffered* signal voltage, and is a result of capacitances of the input pad corresponding to the signal line, ESD circuitry, and the input of the active buffer 202. Noise is injected into the unbuffered signal line from the integrated circuit's substrate V_{SS} through coupling capacitance C_{S1}.

C_{S2} represents coupling capacitance of the *buffered* signal voltage. This capacitance is due primarily to the capacitance of the input of a signal comparator 210 associated with each signal line.

Coupling capacitance associated with the reference voltage includes C_{R1} and C_{R2}. C_{R1} represents coupling capacitance of the *unbuffered*, undistributed reference voltage, and is a result of capacitances of the input pad corresponding to the reference line, ESD circuitry, and the input of the active buffer 204. Noise is injected into the unbuffered reference line from the integrated circuit's substrate V_{SS} through coupling capacitance C_{R1}.

C_{S2} represents coupling capacitance of the *buffered* and distributed reference voltage. This capacitance is due primarily to the capacitance of the input of signal comparator 210.

In this circuit, C_{S1} is approximately equal to C_{R1}. Thus, any noise injected through these capacitances will be common mode. However, C_{R2} is significantly greater than C_{S2}, due to the multitude of signal comparators whose inputs receive the buffered reference voltage. Noise injected through these capacitances tends to contain non-common mode components. However, such non-common mode noise can be greatly reduced by designing the active buffer associated with the reference line with much larger transistors than the active buffers associated with the data signal lines. Specifically, active buffer 204 is designed to have an electrical current capacity that is greater than the electrical current capacity of active buffer 202 by a ratio equal to the ratio of C_{R2} to C_{S2}.

A larger buffer will usually have a higher input capacitance, which will tend to make C_{R1} greater than C_{S1}. However, C_{R1} and C_{S1} are typically dominated by ESD components so that the input capacitances of the active buffers have only negligible effect. Furthermore, the signal line inputs can employ dummy capacitors to equalize C_{R1} and C_{S1}.

Fig. 7 illustrates a third embodiment, appropriate for use in conjunction with two-stage input receivers. This embodiment comprises a plurality of two-stage input receivers 302, and a reference receiver or buffer 304. Input inductance and capacitance are represented in Fig. 7 as L_I and C_I, respectively. The circuit receives a plurality of signal voltages V_{SIGEXT}, which are subject to input inductance L_I and capacitance C_I to produce internal signal voltages referred to as V_{SIG}. The circuit also receives a voltage reference signal V_{REF}, which similarly subject to input inductance L_I and capacitance C_I to produce internal reference voltages referred to as V_{REFU} and V_{REFD}.

The first stage of a two-stage input receiver typically performs signal conditioning such as filtering, translating the input levels from the allowable input common-mode range to a fixed-output common-mode voltage, and converting the single-ended input into a differential output for the second stage. The second stage typically provides gain and performs latching.

In the circuit shown in Fig. 7, a two-stage input receiver 302 is provided for each incoming signal line. A first stage 310 of a receiver receives both a signal voltage V_{SIG} and a distributed reference voltage V_{REFD}. The term "distributed" in this context means that the reference voltage is provided to a plurality of receivers. First stage 310 conditions the signals and determines the voltage differential between them. This voltage differential is then provided to a second stage 312, in the form of a buffered differential voltage V_{BUF1}.

Reference receiver 304 has characteristics similar to first stages 310. Specifically, it has a similar or identical input impedance. In many cases, it is a duplicate of the circuits used within first stages 310.

Reference receiver 304 receives the distributed voltage V_{REFD}, and an undistributed voltage V_{REFU}. V_{REFU} is a voltage or signal that has not been distributed to all of the signal receivers. In this embodiment, the undistributed reference voltage is connected to only to the single reference receiver 304.

The reference receiver is similar to the first stages 310 of the signal receivers and performs similar functions. Specifically, it produces a buffered differential voltage or signal V_{BUF2}, based on the voltage differential between its two inputs—between V_{REFD} and V_{REFU}.

In operation, each V_{SIG} is subject to a load equal to the sum of the signal line impedance (L_I and C_I) and the input impedance of first stage receiver 310. V_{REFD}, however, is additionally subject to a load equal to sum of the signal line impedance (L_I and C_I) and the cumulative input impedance of *all* the first stage receivers 310. Because of this, noise is not produced equally in the distributed reference voltage V_{REFD} as compared to each of the signal voltages V_{SIG}. In other words, the difference between V_{SIG} and V_{REFD} will have a noise component equal to the difference in noise between the signal voltage V_{SIG} and the distributed reference voltage V_{REFD}. V_{REFU}, on the other hand, is subject to the load of only a single receiver 304, just as the signal lines V_{SIG}.

The circuit of Fig. 6 works by generating a buffered voltage V_{BUF2}, which is based at least in part on undistributed reference voltage V_{REFU}. Specifically, V_{BUF2} is equal to V_{REFD} minus V_{REFU}: the difference between the relatively unloaded reference voltage V_{REFU} as it is received and the more heavily loaded reference voltage V_{REFD} after it is distributed to all of the input receivers 310. It also represents the difference between the induced noise on V_{SIG} and the averaged induced noise present on V_{REFD}.

To produce V_{BUF2}, both V_{REFD} and V_{REFU} are connected to the inputs of reference receiver 304, which compares the two voltages and produces V_{BUF2}. V_{BUF2} is distributed to the second stage 312 of each signal receiver 302. In addition, the second stage receives the voltage produced by the first stage of the signal receiver. To correct for noise, the second stage is configured to subtract V_{BUF1} from V_{BUF2}. This results in a noise-compensated output voltage V_{OUT}.

Additional noise and signal degradation in V_{BUF2} are avoided by the use of a differential output from reference receiver 304. First stage 310 also generates a differential output, which avoids additional noise on V_{BUF2}. In addition, receivers 304 and 310 produce sampled outputs, so that the bandwidth of the amplifier driving the noise signal is less critical—one can allocate some time for this amplifier to settle.

A feature of this embodiment is that the noise (V_{BUF2}) is not distributed as a full amplitude signal, equal to the reference voltage plus the noise. Rather, V_{BUF2} in this embodiment represents only noise, and has much smaller amplitude than the summed amplitude V_{BUF} of the previous embodiments.

The circuits described above improve the performance of pseudo-differential signals, allowing smaller voltage differentials to be utilized so that higher switching speeds can be attained.

Although the description above uses language that is specific to structural features and/or methodological acts, it is to be understood that the invention defined in the appended claims is not limited to the specific features or acts described. Rather, the specific features and acts are disclosed as exemplary forms of implementing the invention.

CLAIMS

1. An apparatus that uses pseudo-differential voltage signaling, comprising:

a reference receiver that receives an undistributed reference voltage and in response produces a buffered voltage that is derived at least in part from the undistributed reference voltage;

signal receivers associated respectively with a plurality of signal voltages;

wherein an individual signal receiver receives both its associated signal voltage and the buffered voltage, and;

wherein said individual signal receiver evaluates its associated signal voltage and the buffered voltage to produce an output voltage.

2. An apparatus as recited in claim 1, wherein said individual signal receiver evaluates by comparing the associated signal voltage and the buffered voltage to produce an output voltage.

3. An apparatus as recited in claim 1, wherein the buffered voltage is the difference between the undistributed reference voltage and a distributed reference voltage.

4. An apparatus as recited in claim 1, wherein the buffered voltage is proportional to the undistributed reference voltage.

5. An apparatus as recited in claim 1, wherein the buffered voltage represents the noise of the signal voltages relative to the undistributed reference voltage.

6. An apparatus as recited in claim 1, wherein the reference receiver also receives a distributed reference voltage that is received by the signal receivers, wherein the reference receiver is responsive to the distributed reference voltage and the undistributed reference voltage to produce the buffered voltage.

7. An apparatus as recited in claim 1, wherein the reference receiver also receives a distributed reference voltage that is received by the signal receivers, wherein the reference receiver compares the distributed reference voltage and the undistributed reference voltage to produce the buffered voltage.

8. An apparatus as recited in claim 1, wherein the reference receiver also receives a distributed reference voltage that is received by the signal receivers, wherein the reference receiver compares the distributed reference voltage and the undistributed reference voltage to produce the buffered voltage, the buffered voltage representing the difference between the distributed reference voltage and the undistributed reference voltage.

9. An apparatus as recited in claim 1, further comprising:

a plurality of signal buffers that receive the signal voltages and in response produce buffered signal voltages, wherein each buffered signal voltage is subject to a signal capacitance;

the buffered voltage being subject to a reference capacitance that is significantly greater than the signal capacitance;

each of the signal buffers having a first electrical current capacity;

the reference receiver having a second electrical current capacity that is greater than the first electrical current capacity by a ratio equal to the ratio of the reference capacitance to the signal capacitance.

10. An apparatus as recited in claim 1, further comprising:

a plurality of signal buffers that receive the signal voltages and in response produce buffered signal voltages, wherein each buffered signal voltage is subject to a signal capacitance;

the buffered voltage being subject to a reference capacitance that is significantly greater than the signal capacitance;

each of the signal buffers having a first electrical current capacity;

the reference receiver having a second electrical current capacity that is greater than the first electrical current capacity by a ratio equal to the ratio of the reference capacitance to the signal capacitance; and

wherein the reference receiver and the signal buffers are source-followers.

11. An apparatus as recited in claim 1, further comprising:

a plurality of signal buffers that receive the signal voltages and in response produce buffered signal voltages.

12. An apparatus as recited in claim 1, further comprising:

a plurality of signal buffers that receive the signal voltages and in response produce buffered signal voltages;

wherein the reference receiver and the signal buffers are source-followers.

13. An apparatus as recited in claim 1, wherein the reference receiver has a unity gain.

14. An apparatus as recited in claim 1, wherein:

the signal voltage has associated input capacitance and inductance that result in a resonant input frequency;

the reference receiver has a bandwidth that is significantly greater than the resonant input frequency.

15. An apparatus as recited in claim 1, wherein:

the signal voltage has associated input capacitance and inductance that result in a resonant input frequency;

the reference receiver has a bandwidth of at least ten times the resonant input frequency.

16. An apparatus as recited in claim 1, wherein each signal voltage represents one of two values and the signal receivers compare the buffered voltage and the signal voltages to determine which of the two values is represented by each signal voltage.

17. An apparatus as recited in claim 1, the reference voltage and the buffered voltage being subject to similar impedances.

18. An apparatus as recited in claim 1, the reference voltages and signal voltage being subject to similar impedances, wherein coupled signal noise is introduced approximately equally in the buffered voltage and the plurality of pseudo-differential signal voltages, said approximately equal coupled signal noise being canceled in the evaluation performed by the signal receiver.

19. An integrated circuit comprising:

a reference input that receives a common reference voltage;

a plurality of signal inputs configured to receive pseudo-differential signal voltages that represent values in terms of relationships between the pseudo-differential signal voltages and the common reference voltage;

a reference buffer that receives the common reference voltage and in response produces a buffered reference voltage;

signal comparators associated respectively with the plurality of pseudo-differential signal voltages, each signal comparator comparing the buffered reference voltage and one of the pseudo-differential signal voltages to determine the value represented by said one of the pseudo-differential signal voltages;

wherein the reference and signal inputs have similar impedances, coupled signal noise being introduced approximately equally in the buffered reference voltage and the plurality of pseudo-differential signal voltages, said approximately equal coupled signal noise being canceled in the comparison performed by the signal comparators.

20. An integrated circuit as recited in claim 19, further comprising:

a plurality of signal buffers that receive the pseudo-differential signal voltages and in response produce buffered signal voltages, wherein each buffered signal voltage is subject to a signal capacitance;

the buffered reference voltage being subject to a reference capacitance that is significantly greater than the signal capacitance;

each of the signal buffers having a first electrical current capacity;

the reference buffer having a second electrical current capacity that is greater than the first electrical current capacity by a ratio equal to the ratio of the reference capacitance to the signal capacitance.

21. An integrated circuit as recited in claim 19, further comprising:

a plurality of signal buffers that receive the pseudo-differential signal voltages and in response produce buffered signal voltages, wherein each buffered signal voltage is subject to a signal capacitance;

the buffered reference voltage being subject to a reference capacitance that is significantly greater than the signal capacitance;

each of the signal buffers having a first electrical current capacity;

the reference buffer having a second electrical current capacity that is greater than the first electrical current capacity by a ratio equal to the ratio of the reference capacitance to the signal capacitance; and

wherein the reference buffer and the signal buffers are source-followers.

22. An integrated circuit as recited in claim 19, further comprising:

a plurality of signal buffers that receive the pseudo-differential signal voltages and in response produce buffered signal voltages for comparison by the signal comparators.

23. An integrated circuit as recited in claim 19, further comprising:

a plurality of signal buffers that receive the pseudo-differential signal voltages and in response produce buffered signal voltages;

wherein the reference buffer and the signal buffers are source-followers.

24. An integrated circuit as recited in claim 19, wherein the reference buffer has a unity gain.

25. An integrated circuit as recited in claim 19, wherein:

the signal inputs have associated input capacitances and inductances that result in a resonant input frequency;

the reference buffer has a bandwidth that is significantly greater than the resonant input frequency.

26. An integrated circuit as recited in claim 19, wherein:

the signal input has associated input capacitance and inductance that result in a resonant input frequency;

the reference buffer has a bandwidth of at least ten times the resonant input frequency.

27. An integrated circuit as recited in claim 19, wherein each signal voltage represents one of two values and the signal comparators compare the buffered reference voltage and the signal voltages to determine which of the two values is represented by each signal voltage.

28. An integrated circuit as recited in claim 19, the reference and signal inputs having matching impedances.

29. A system comprising:

a first integrated circuit that transmits a common reference voltage and a plurality of pseudo-differential signal voltages, wherein the pseudo-differential signal voltages represent values in terms of relationships between the pseudo-differential signal voltages and the common reference voltage;

a second integrated circuit that receives the common reference voltage and the plurality of pseudo-differential signal voltages;

the second integrated circuit having a reference buffer that receives the common reference voltage and in response produces a buffered reference voltage;

the second integrated circuit having signal comparators associated respectively with the plurality of pseudo-differential signal voltages, each signal comparator comparing the buffered reference voltage and a respective one of the pseudo-differential signal voltages to determine the value represented by said one of the pseudo-differential signal voltages;

wherein the second integrated circuit is configured to introduce approximately equal coupled signal noise in the buffered reference voltage and the plurality of pseudo-differential signal voltages, said approximately equal coupled

signal noise being canceled in the comparisons performed by the signal comparators.

30. A system as recited in claim 29, the second integrated circuit further comprising:

a plurality of signal buffers that receive the pseudo-differential signal voltages and in response produce buffered signal voltages, wherein each buffered signal voltage is subject in the second integrated circuit to a signal capacitance;

the buffered reference voltage being subject in the second integrated circuit to a reference capacitance that is significantly greater than the signal capacitance;

each of the signal buffers having a first electrical current capacity;

the reference buffer having a second electrical current capacity that is greater than the first electrical current capacity by a ratio equal to the ratio of the reference capacitance to the signal capacitance.

31. A system as recited in claim 29, the second integrated circuit further comprising:

a plurality of signal buffers that receive the pseudo-differential signal voltages and in response produce buffered signal voltages, wherein each buffered signal voltage is subject in the second integrated circuit to a signal capacitance;

the buffered reference voltage being subject in the second integrated circuit to a reference capacitance that is significantly greater than the signal capacitance;

each of the signal buffers having a first electrical current capacity;

the reference buffer having a second electrical current capacity that is greater than the first electrical current capacity by a ratio equal to the ratio of the reference capacitance to the signal capacitance; and

wherein the reference buffer and the signal buffers are source-followers.

32. A system as recited in claim 29, the second integrated circuit further comprising:

a plurality of signal buffers that receive the pseudo-differential signal voltages and in response produce buffered signal voltages.

33. A system as recited in claim 29, the second integrated circuit further comprising:

a plurality of signal buffers that receive the pseudo-differential signal voltages and in response produce buffered signal voltages;

wherein the reference buffer and the signal buffers are source-followers.

34. A system as recited in claim 29, wherein the reference buffer is a unity gain amplifier.

35. A system as recited in claim 29, wherein:

the second integrated circuit has signal inputs that receive the plurality of signal voltages, the signal inputs having associated input capacitance and inductance that result in a resonant input frequency;

the reference buffer has a bandwidth that is significantly greater than the resonant input frequency.

36. A system as recited in claim 29, wherein:

the second integrated circuit has signal inputs that receive the plurality of signal voltages, the signal inputs having associated input capacitance and inductance that result in a resonant input frequency;

the reference buffer has a bandwidth of at least ten times the resonant input frequency.

37. A system as recited in claim 29, wherein each pseudo-differential signal voltage represents one of two values and the comparators compare the buffered reference voltage and the pseudo-differential signal voltages to determine which of the two values is represented by each pseudo-differential signal voltage.

38. A system as recited in claim 29, wherein the second integrated circuit has signal inputs that receive the pseudo-differential signal voltages and a reference input that receives the common reference voltage, the reference and signal inputs having similar impedances.

39. A method comprising:

receiving a reference voltage;

receiving a plurality of signal voltages;

producing a buffered voltage based at least in part on the reference voltage;

evaluating the buffered voltage and one of the signal voltages to determine a value represented by said one of the signal voltages.

40. A method as recited in claim 39, wherein the evaluating comprises comparing said one of the signal voltages and the buffered voltage to produce an output voltage.

41. A method as recited in claim 39, wherein the buffered voltage is the difference between an undistributed reference voltage and a distributed reference voltage.

42. A method as recited in claim 39, wherein the buffered voltage is proportional to the reference voltage.

43. A method as recited in claim 39, wherein the buffered voltage represents the noise of the signal voltages.

44. A method as recited in claim 39, said producing comprising comparing a distributed reference voltage that is received by the signal receivers and an undistributed reference voltage that is not received by the signal receivers.

45. A method as recited in claim 39, said producing comprising comparing a distributed reference voltage that is received by the signal receivers and a undistributed reference voltage that is not received by the signal receivers, the buffered voltage representing the difference between the undistributed reference voltage and the distributed reference voltage.

46. A method as recited in claim 39, further comprising:

buffering the signal voltages with signal buffers to produce buffered signal voltages, wherein each buffered signal voltage is subject to a signal capacitance;

said producing the buffered voltage being performed with a reference buffer, the buffered voltage being subject to a reference capacitance that is significantly greater than the signal capacitance;

each of the signal buffers having a first electrical current capacity;

the reference buffer having a second electrical current capacity that is greater than the first electrical current capacity by a ratio equal to the ratio of the reference capacitance to the signal capacitance.

47. A method as recited in claim 39, further comprising:

buffering the signal voltages with source-follower signal buffers to produce buffered signal voltages, wherein each buffered signal voltage is subject to a signal capacitance;

said producing the buffered voltage being performed with a source-follower reference buffer, the buffered voltage being subject to a reference capacitance that is significantly greater than the signal capacitance;

each of the signal buffers having a first electrical current capacity;

the reference buffer having a second electrical current capacity that is greater than the first electrical current capacity by a ratio equal to the ratio of the reference capacitance to the signal capacitance.

48. A method as recited in claim 39, further comprising:

buffering the signal voltages to produce buffered signal voltages.

49. A method as recited in claim 39, further comprising:

buffering the signal voltages with source-followers to produce buffered signal voltages.

50. A method as recited in claim 39, wherein:

the signal voltages are received by signal inputs having associated input capacitances and inductances that define a resonant frequency;

producing the buffered voltage with a unity gain buffer having a bandwidth that is significantly greater than the resonant frequency.

51. A method as recited in claim 39, wherein:

the signal voltages are received by signal inputs having associated input capacitances and inductances that define a resonant input frequency;

producing the buffered voltage with a unity gain buffer having a bandwidth of at least ten times the resonant input frequency.

52. A method as recited in claim 39, wherein:

the reference voltage is received by a reference input;

the signal voltages are received by signal inputs; and

the reference and signal inputs have similar impedances.

53. A method as recited in claim 39, further comprising introducing coupled signal noise approximately equally in the buffered reference voltage and the plurality of signal voltages, said approximately equal coupled signal noise being canceled in the comparing.

54. An apparatus that uses pseudo-differential voltage signaling, comprising:

signal receivers associated respectively with a plurality of signal voltages;

a reference receiver that receives both an undistributed reference voltage and a distributed reference voltage, wherein the distributed reference voltage is distributed to the signal receivers and the undistributed reference voltage is not distributed to the signal receivers;

wherein the reference receiver evaluates the undistributed reference voltage and the distributed reference voltage to produce a buffered voltage that represents the difference between the undistributed reference voltage and the distributed reference voltage;

wherein an individual signal receiver receives both its associated signal voltage and the buffered voltage; and

wherein said individual signal receiver adjusts its associated signal voltage by the buffered voltage to produce an output voltage.

55. An apparatus as recited in claim 54, wherein said signal receivers are two-stage receivers.

56. An apparatus as recited in claim 54, wherein said signal receivers are two-stage receivers, the second stage of the receivers adjusting the signal voltages.

57. An apparatus as recited in claim 54, wherein the buffered voltage represents the noise of the signal voltages relative to the undistributed reference voltage.

58. An apparatus as recited in claim 54, wherein the buffered voltage is a differential voltage.

59. An integrated circuit that uses pseudo-differential voltage signaling, comprising:

two-stage receivers associated respectively with a plurality of signal voltages;

a reference receiver that receives both an undistributed reference voltage and a distributed reference voltage, wherein the distributed reference voltage is distributed to the signal receivers and the undistributed reference voltage is not distributed to the signal receivers;

wherein the reference receiver compares the undistributed reference voltage and the distributed reference voltage to produce a buffered voltage that represents the difference between the undistributed reference voltage and the distributed reference voltage;

wherein the first stage of an individual signal receiver compares its associated signal voltage to the distributed reference voltage to produce a voltage differential signal; and

wherein the second stage of said individual two-stage receiver adjusts the voltage differential signal by the buffered voltage to produce an output voltage.

60. An apparatus as recited in claim 59, the two-stage receiver has an input impedance similar to that of the reference receiver.

61. An apparatus as recited in claim 59, wherein the buffered voltage represents the noise of the signal voltages relative to the undistributed reference voltage.

62. An apparatus as recited in claim 59, wherein the buffered voltage is a differential voltage.

63. A system comprising:

a first integrated circuit that transmits a common reference voltage and a plurality of pseudo-differential signal voltages, wherein the pseudo-differential signal voltages represent values in terms of relationships between the pseudo-differential signal voltages and the common reference voltage;

a second integrated circuit that receives the common reference voltage and the plurality of pseudo-differential signal voltages;

the second integrated circuit having a reference receiver that receives the common reference voltage and in response produces a buffered voltage;

the second integrated circuit having two-stage signal receivers associated respectively with the plurality of pseudo-differential signal voltages, each two-stage signal receiver adjusting one of the pseudo-differential signal voltages by the buffered voltage to produce an output voltage.

64. A system as recited in claim 63, wherein each two-stage signal receiver has an input impedance similar to that of the reference receiver.

65. A system as recited in claim 63, wherein:

the reference receiver compares a distributed common reference voltage to an undistributed common reference voltage to produce the buffered voltage;

the first stage of an individual two-stage signal receiver compares its associated pseudo-differential signal voltage to a distributed reference voltage to produce a voltage differential signal; and

the second stage of said individual two-stage signal receiver adjusts the voltage differential signal by the buffered voltage to produce an output voltage.

66. A system as recited in claim 63, wherein the buffered voltage represents the noise of the signal voltages.

67. A system as recited in claim 63, wherein the buffered voltage is a differential voltage.

ABSTRACT

A pseudo-differential signaling system uses a plurality of signal lines and a single, common reference voltage. Signal line voltages are interpreted only in comparison to the reference line voltage. Within a receiving circuit, the reference line is buffered prior to its distribution to multiple comparators. The system utilizes an active buffer having a bandwidth that is significantly greater than the resonant input frequency of the receiving circuit. In an alternative embodiment, the signal lines are also buffered. In this embodiment, the buffers are implemented with transistor-based source-followers. The buffer associated with the reference line has a larger current capacity than the buffers associated with the signal lines. In yet another embodiment, a comparator produces a correction signal that is equal to the noise present on the signal lines. This noise is then subtracted from the signal voltages.

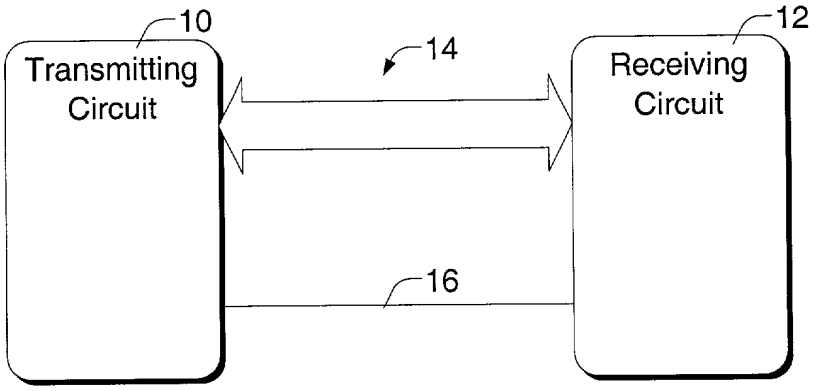

Fig. 1
Prior Art

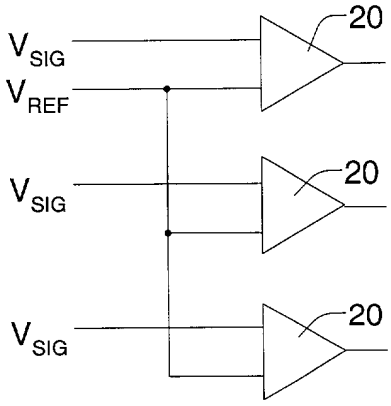

Fig. 2
Prior Art

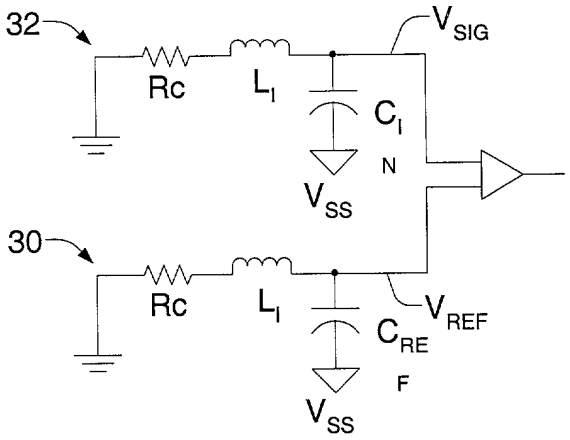

Fig. 3

Prior Art

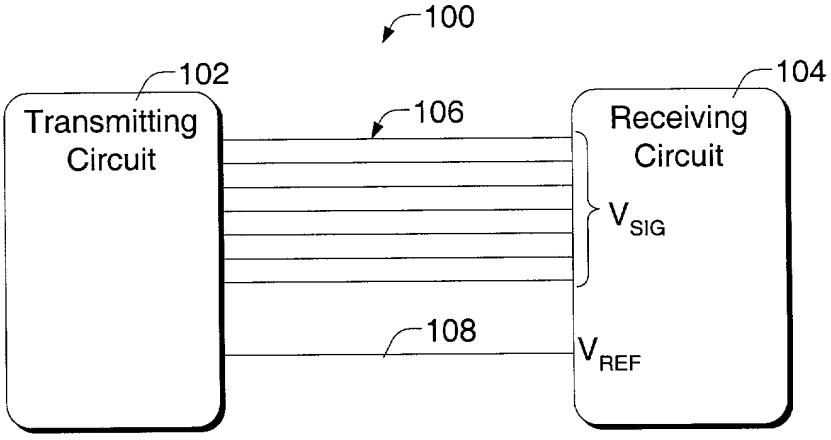

Fig. 4

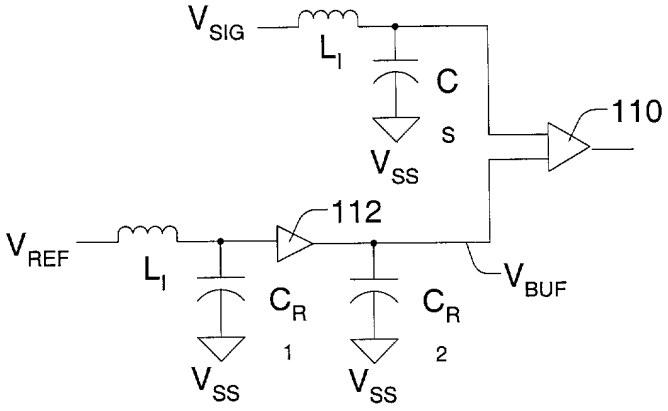
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Fig. 5

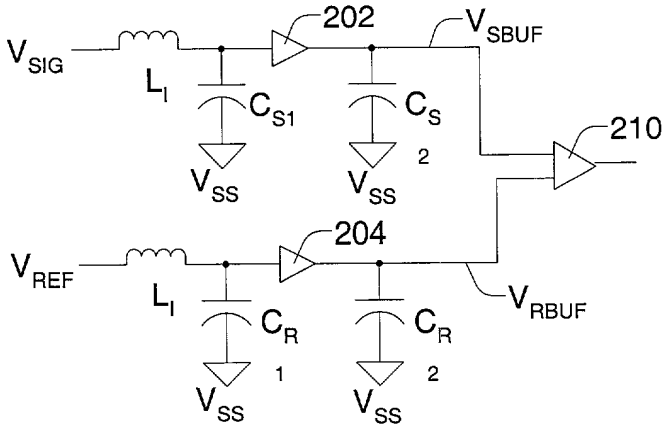
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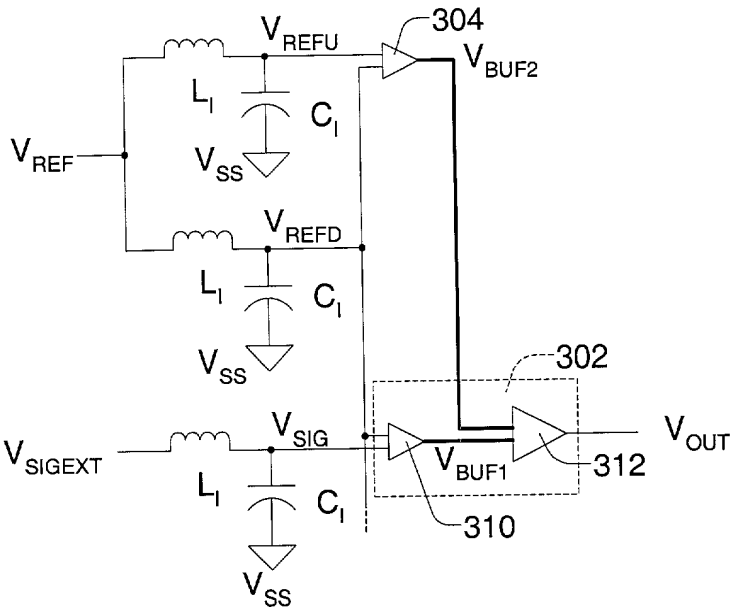
Fig. 6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310
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Fig. 7

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventorship ..... Sidiropoulos et al.
Applicant..... Rambus Inc.
Attorney's Docket No. RB1-005US
Title: Reducing Coupled Noise in Pseudo-Differential Signaling Systems

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled "Reducing Coupled Noise in Pseudo-Differential Signaling Systems," the specification of which is attached hereto.

I have reviewed and understand the content of the above-identified specification, including the claims.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

PRIOR FOREIGN APPLICATIONS: no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

Power of Attorney

I appoint the following attorneys to prosecute this application and transact all future business in the Patent and Trademark Office connected with this application: Lewis C. Lee, Reg. No. 34,656; Daniel L. Hayes, Reg. No. 34,618; Allan T.

Sponseller, Reg. 38,318; Steven R. Sponseller, Reg. No. 39,384; James R. Banowsky, Reg. No. 37,773; Lance R. Sadler, Reg. No. 38,605; Michael A. Proksch, Reg. No. 43,021; Thomas A. Jolly, Reg. No. 39,241; Kasey C. Christie, Reg. No. 40,559 and David A. Morasch, Reg. No. 42,905.

Send correspondence to: LEE & HAYES, PLLC, 421 W. Riverside Avenue, Suite 500, Spokane, Washington, 99201. Direct telephone calls to: Daniel L. Hayes (509) 324-9256.

All statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statement may jeopardize the validity of the application or any patent issued therefrom.

* * * * * * * * * *

Full name of inventor:	Stefanos Sidiropoulos
Inventor's Signature	_____ Date: 11/6/2000
Residence:	Palo Alto, CA
Citizenship:	Greece
Post Office Address:	731 Ellsworth Street Palo Alto, CA 94306

* * * * * * * * * *

Full name of inventor: Yingxuan Li

Inventor's Signature _____ Date: 11/6/00

Residence: Cupertino, CA

Citizenship: China

Post Office Address: 902 Cottonwood Drive
Cupertino, CA 95014

* * * * * * * * * *

Full name of inventor: Mark A. Horowitz

Inventor's Signature _____ Date: Nov 3, 2000

Residence: Menlo Park, CA

Citizenship: USA

Post Office Address: 1309 San Mateo Drive
Menlo Park, CA 94025